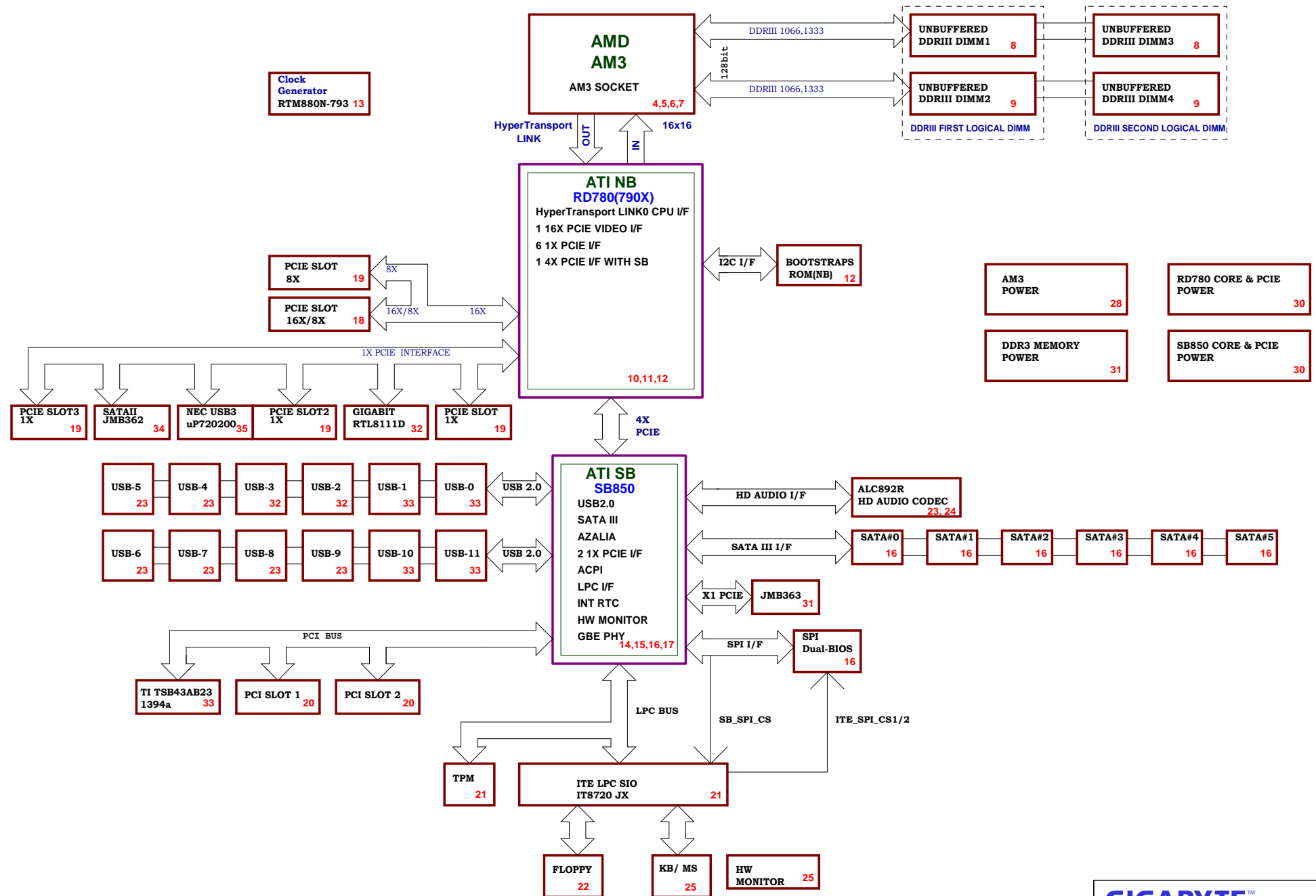


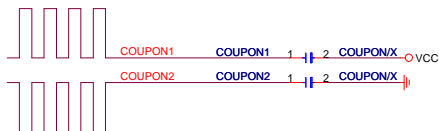
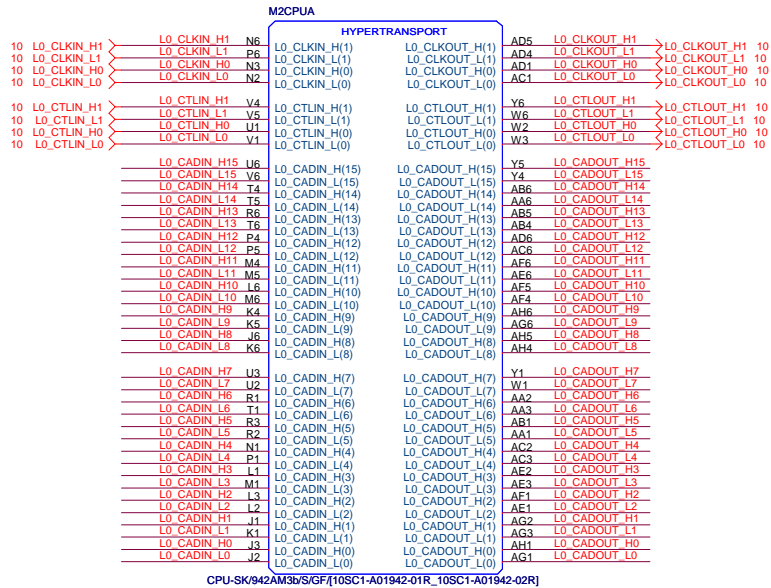
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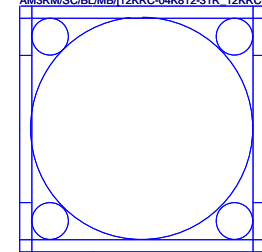


CPU_VDD_RUN = VCORE
 CPU_VDDA_RUN = VDDA25
 VLDT_RUN = VCC12_HT
 CPU_VDDIO_SUS = DDR15V
 CPU_VDDR = CPU_VDDR12

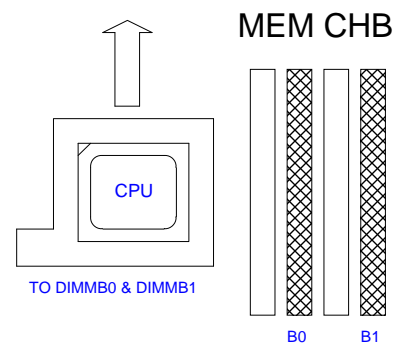
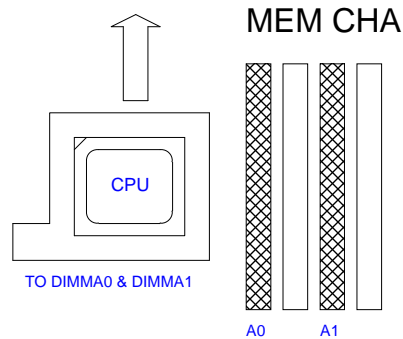
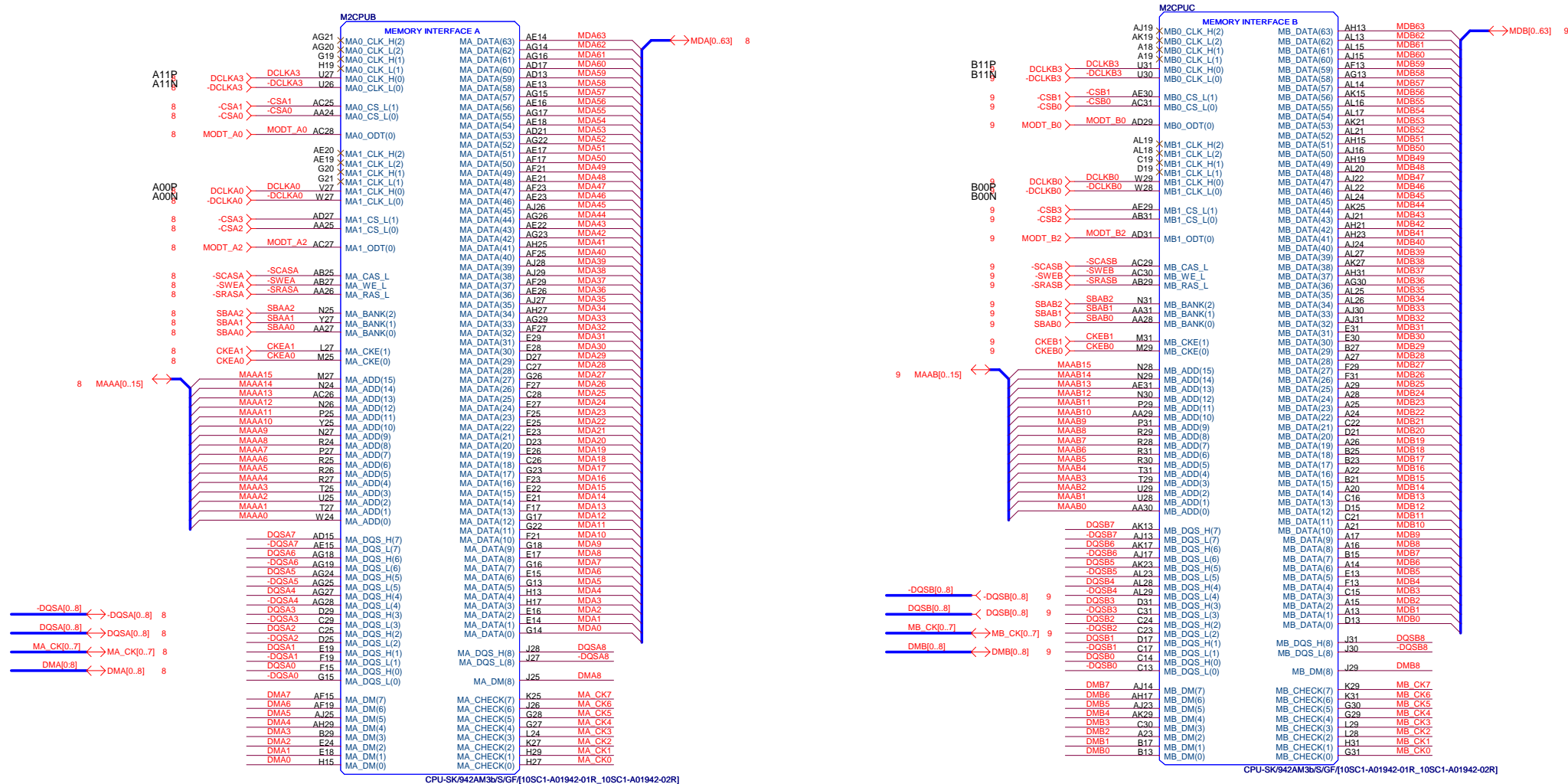
VLDT_A = VCC12_HT
 VLDT_B = HT12B

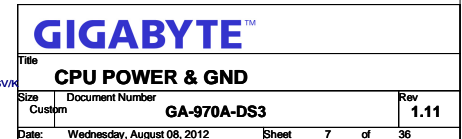


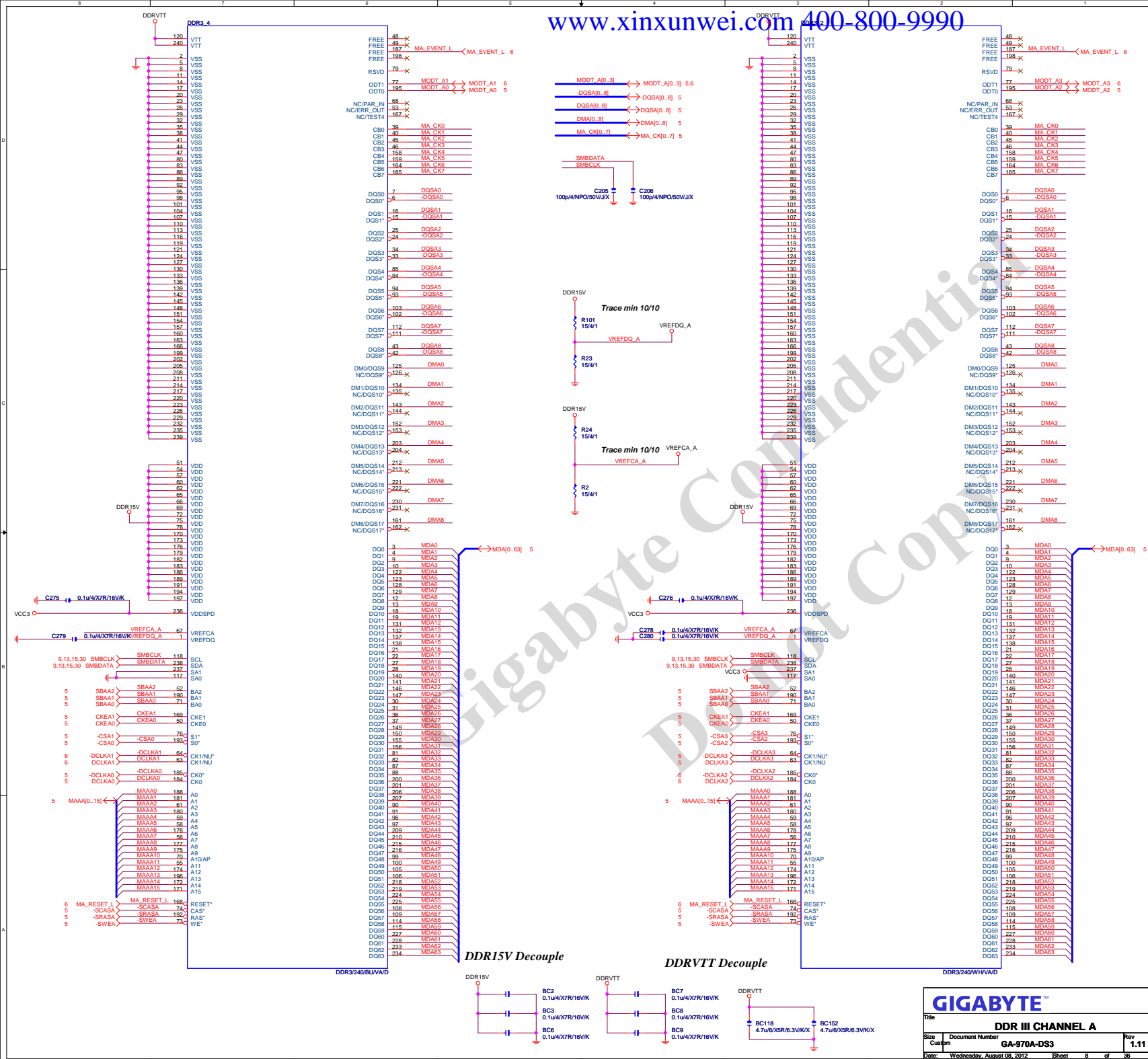
M2CPU
 AM3RM/SC/BLMB/12KRC-04K812-31R_12KRC-04K812-32R]

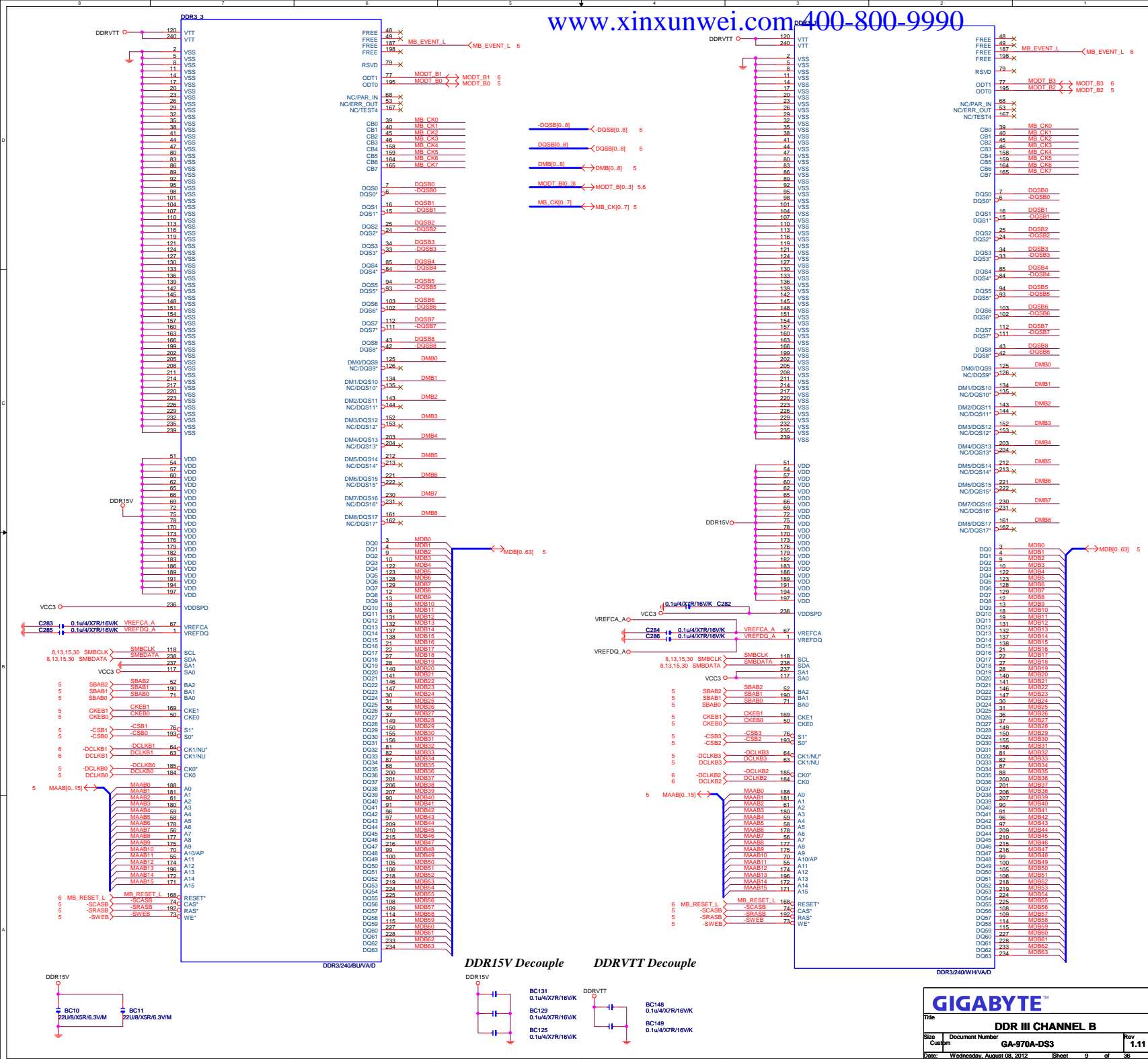


GIGABYTE™			
Title			
CPU HYPER TRANSPORT			
Size	Document Number	Rev	
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Date:	Wednesday, August 08, 2012	Sheet	4 of 36









U3A

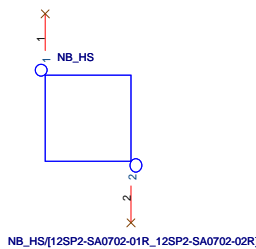
PART 1/5

HYPERTRANSPORT IF

RX980/BGA692

L0_CADIN_L[0..15] <L0_CADIN_L[0..15] 4
 L0_CADIN_H[0..15] <L0_CADIN_H[0..15] 4

L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] 4
 L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] 4

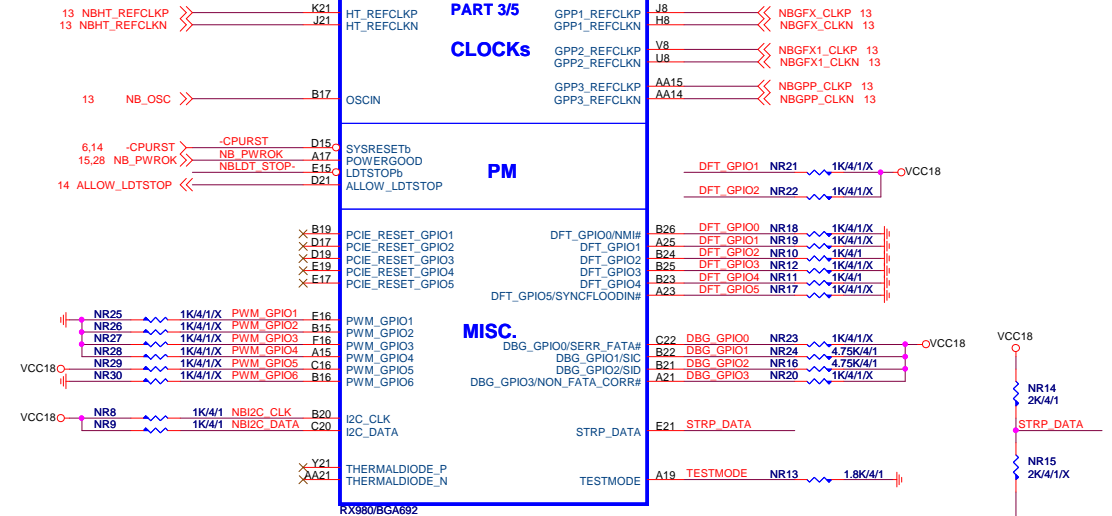


U3C

PART 3/5
CLOCKS

PM

MISC.



DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLEB

Enables the Test Debug Bus using GPIO.
 1 : Disable (Can still be enabled using nbcfg register access)
 0 : Enable

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.
 GPIO4:3:2
 000 : 4:2:4 B
 001 : 4:1:1:4 C
 010 : 1:1:1:1:1:4 L (Hardware Default)
 011 : 2:1:1:1:1:4 E
 100 : 2:2:1:1:4 K
 101 : 2:2:2:4 C2
 110: Hardware default (mode L) or EEPROM
 111: Hardware default (mode L) or EEPROM
 101 : 01100
 111 : 01011

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLED

Enables the Test Debug Bus using PCIE bus
 1 : Disable (Can still be enabled using nbcfg register access)
 0 : Enable

GIGABYTE™

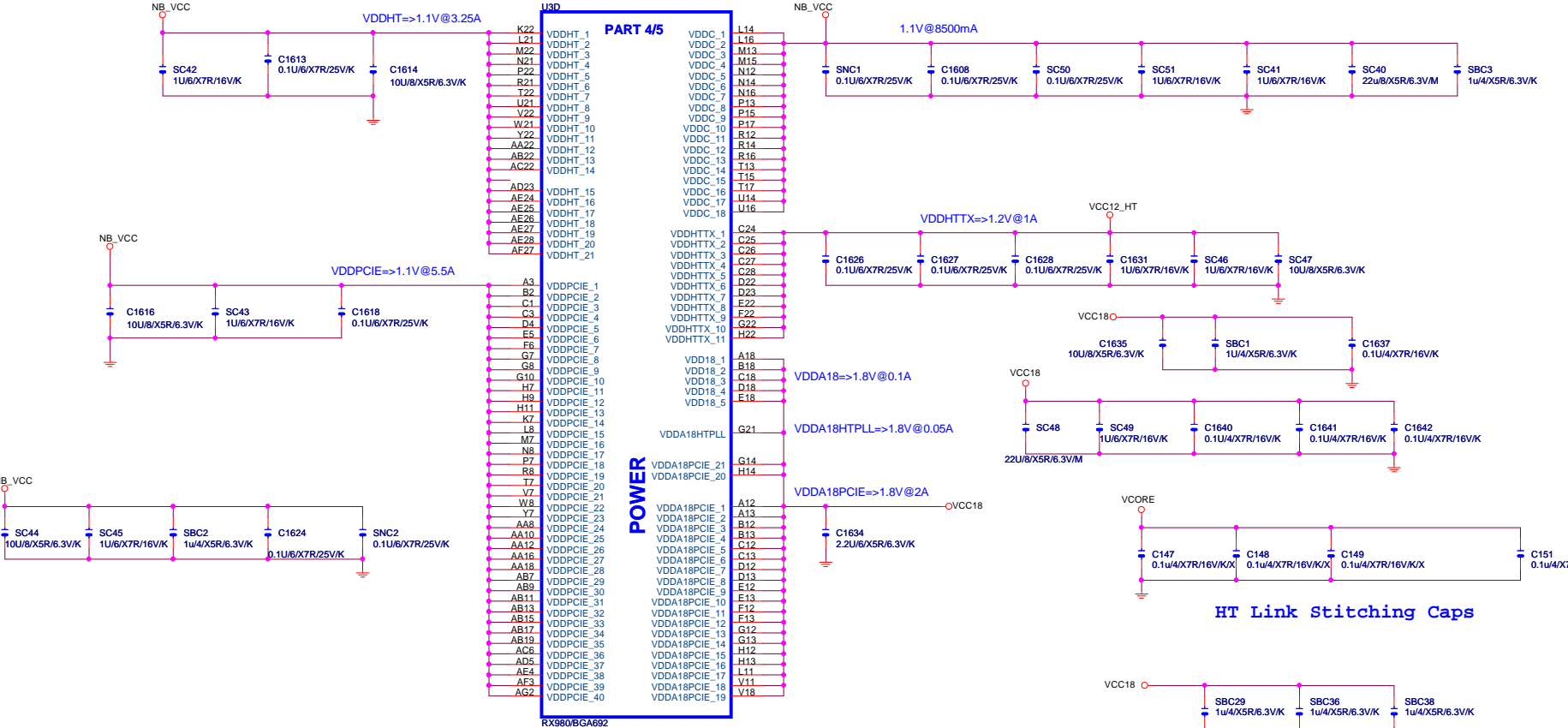
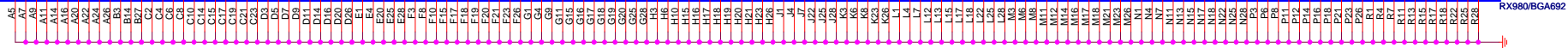
Title RS780 HT-LINK V/F

Size Custom Document Number GA-970A-DS3 Rev 1.11

Date: Wednesday, August 08, 2012 Sheet 10 of 36

PART 5/5

GROUND



NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

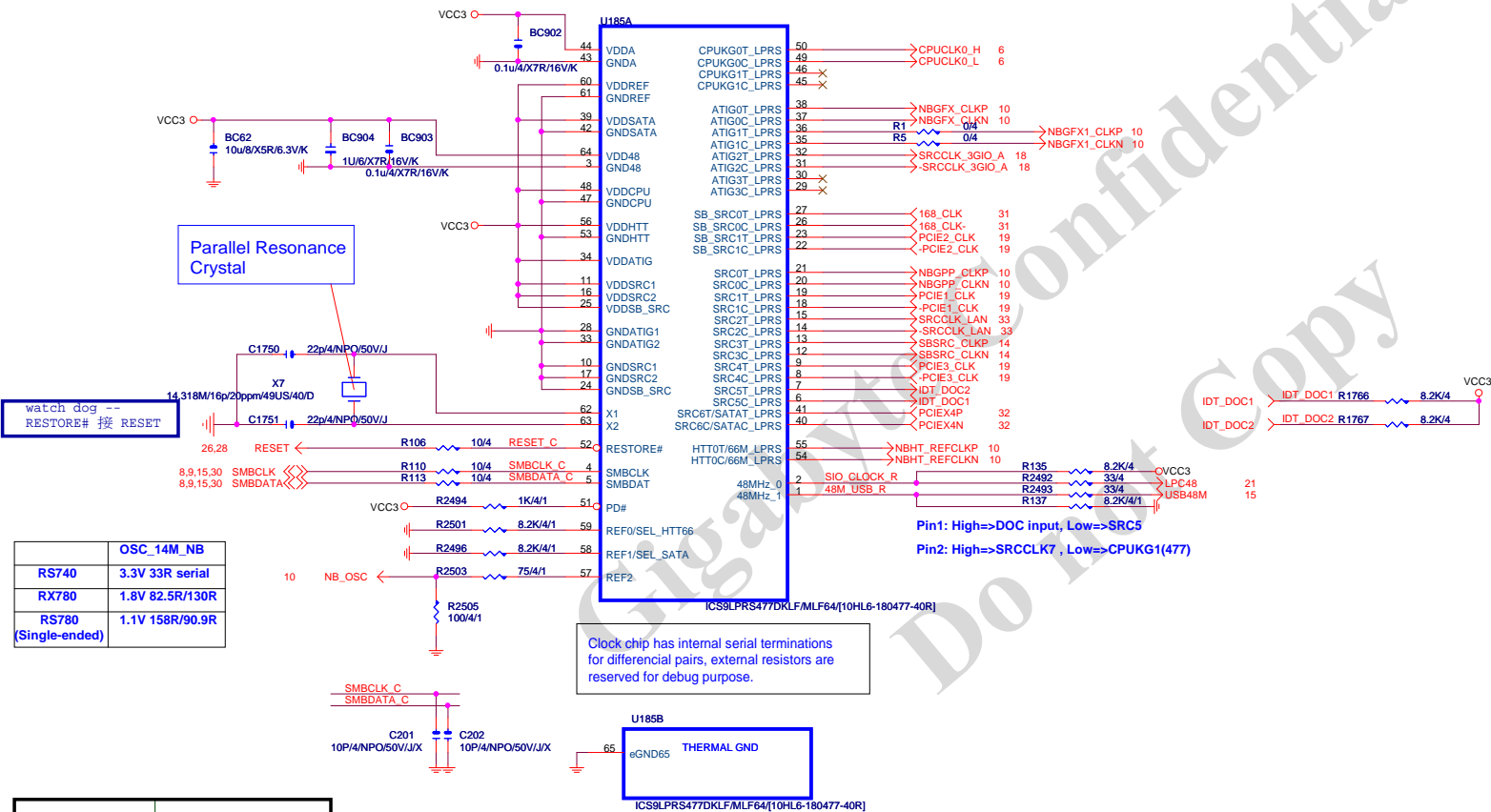
* the GFX_REFCLK input is required for all cases

1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE

2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE

3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair



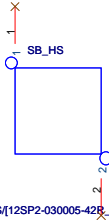
GIGABYTE™

Title
RTM880N-793Size
Custom
Document Number
GA-970A-DS3
Rev
1.11

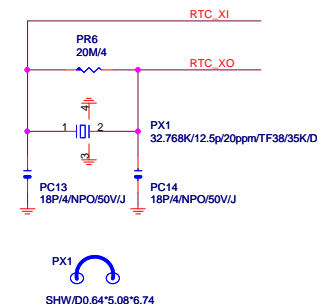
Date: Wednesday, August 08, 2012 Sheet 13 of 36

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850

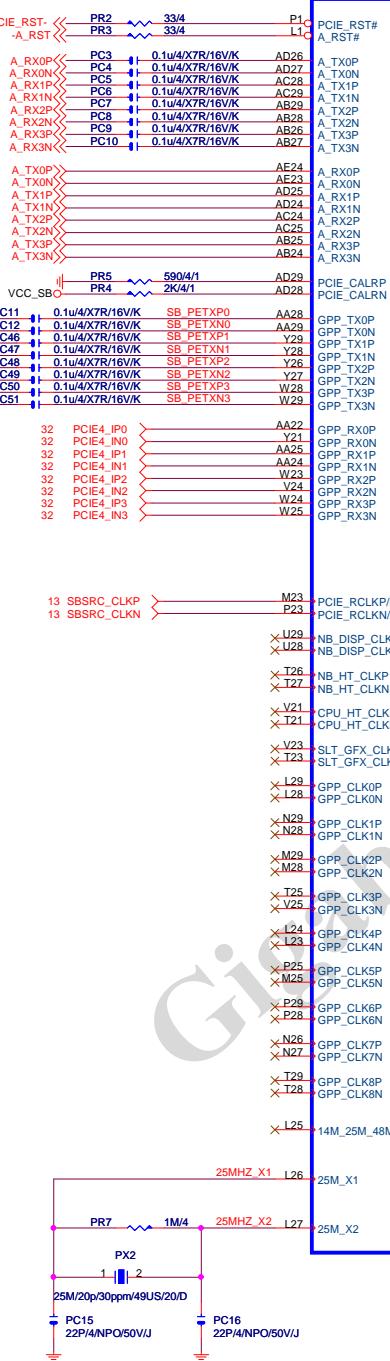
S.B HEATSINK



SB_HS/[12SP2-030005-42R_12SP2-030005-43R]



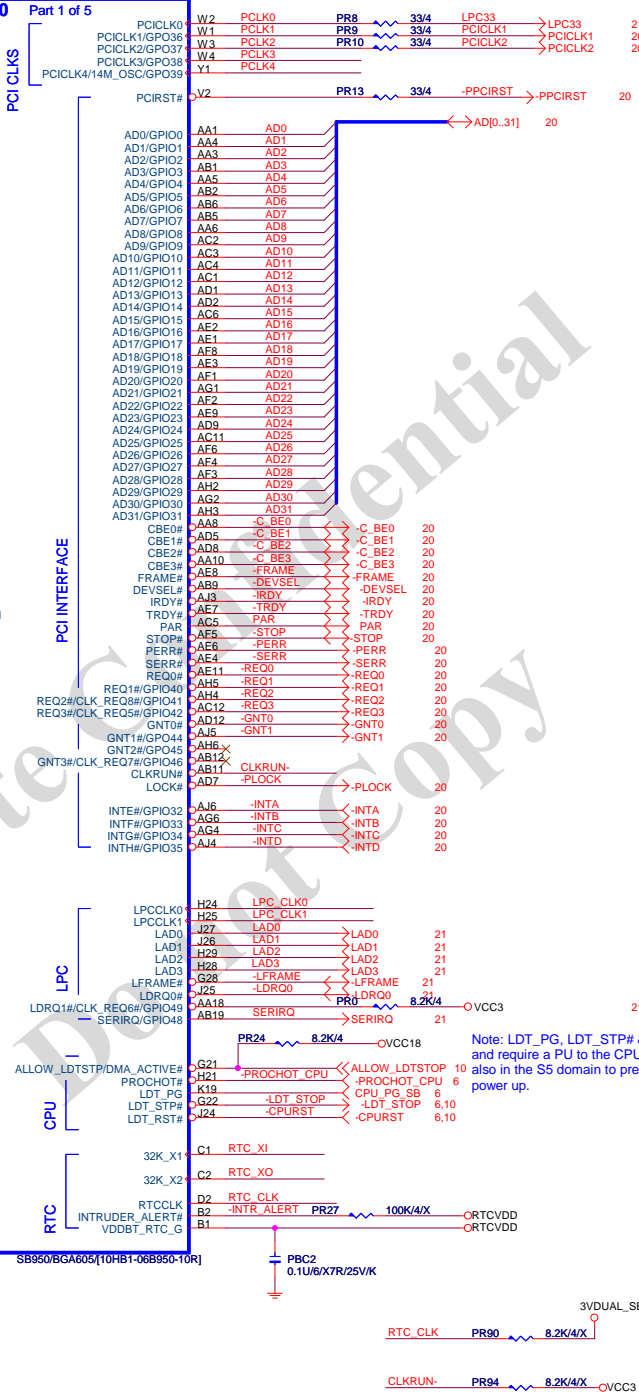
SHW/D0.64*5.08*6.74



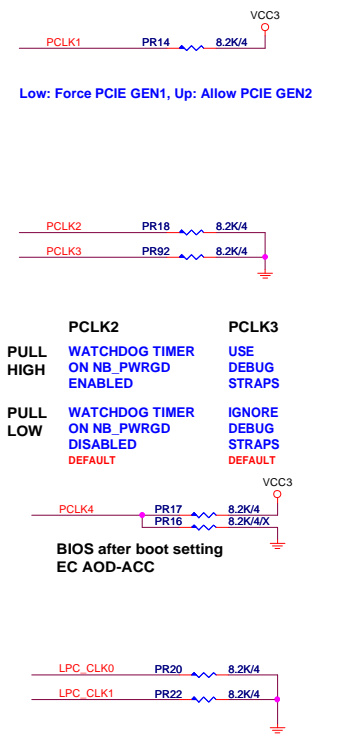
PCI EXPRESS INTERFACES

PCI INTERFACE

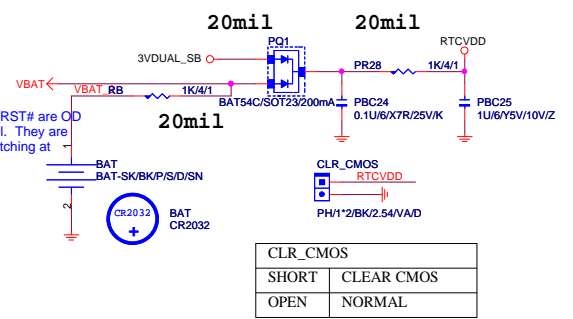
CLOCK GENERATOR




Note: LDT_PG, LDT_STP# & LDT_RST# are
and require a PU to the CPU I/O rail. They a
also in the S5 domain to prevent glitching at
power up.

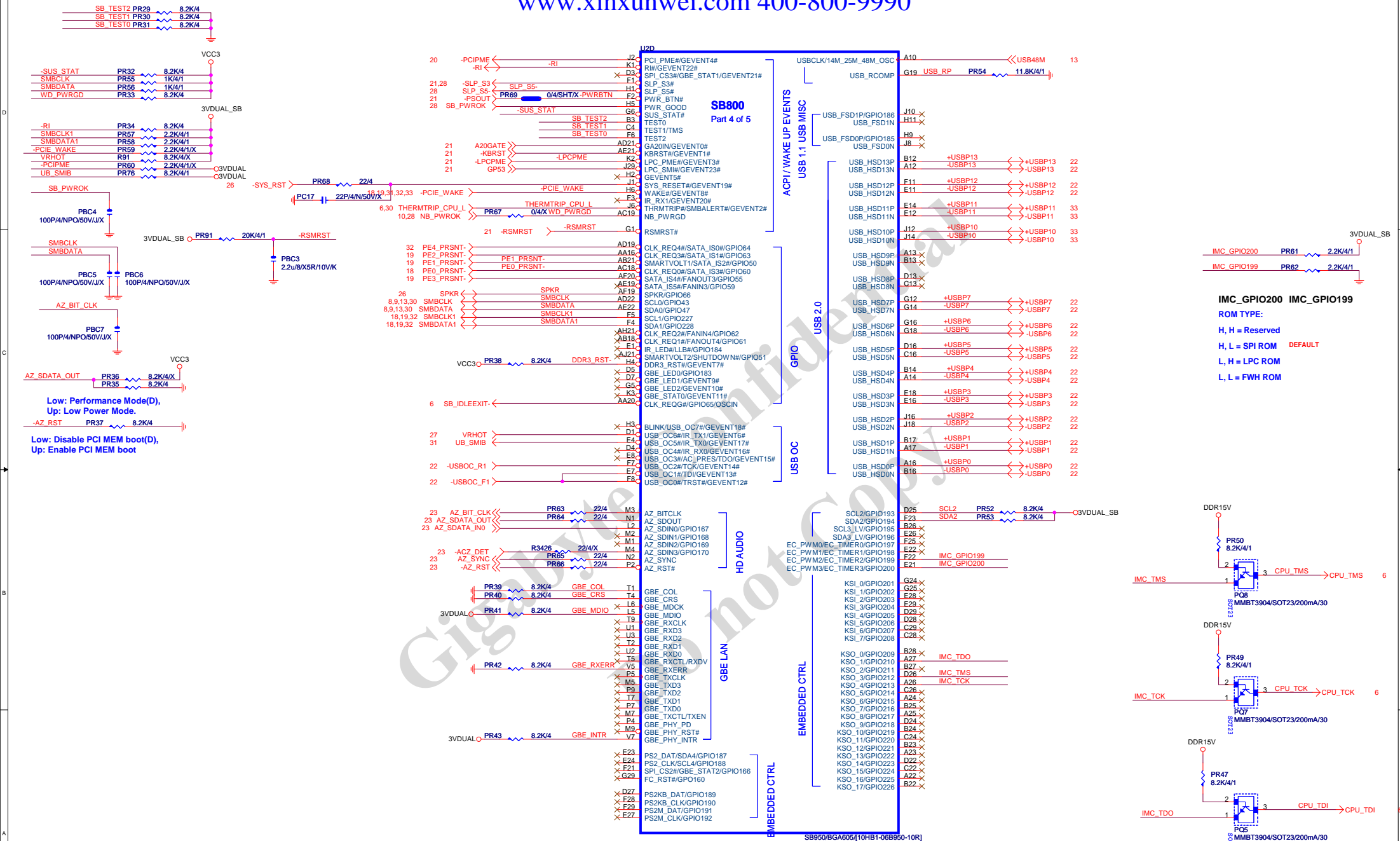


	LPC_CLK0 Rev.A12	LPC_CLK1
PULL	IMC	CLKGEN
HIGH	ENABLED	ENABLED
	AOD Extreme	
PULL	IMC	CLKGEN
LOW	DISABLED	DISABLED
	DEFAULT	DEFAULT



NOT ADD ICT FOR RTCVDD PIN

			
Title			
ATI SB700 PCIE/PCI/CPU/LPC			
Size	Document Number	Rev	
Custom	GA-970A-DS3	1.11	
Date:	Wednesday, August 08, 2012	Sheet	14 of 36





PLACE SATA CAL
RES VERY CLOSE
TO BALL OF U600

NOTE:

R650 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

VCC_SB0 PR75 1K/4/1 SATA_CALRP AB14
PR74 931/4/1 SATA_CALRN AA14

26 -SATA_LED -SATA_LED AD11

TP5 -SATA_X1 AD16

TP7 -SATA_X2 AC16

SB SPI DI PR70 22/4 SB SPI DI_R J5
SB SPI DO PR71 22/4 SB SPI DO_R F2
SB SPI CLK PR72 22/4 SB SPI CLK_R K4
SB SPI CS_ITE PR73 22/4 SB SPI CS_ K9
SB SPI CS_ITE PR73 22/4 SB SPI CS_ K9

SB950/BGA605(10HB1-06B950-10R)



PLACE SATA AC COUPLING
CAPS CLOSE TO SB850

SERIAL ATA

HW MONITOR

SPIROM

SB800
Part 2 of 5

GPIO

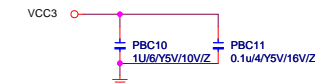
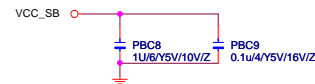
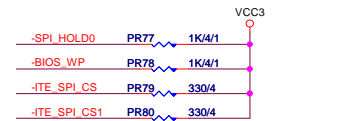
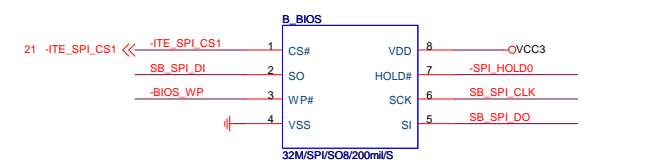
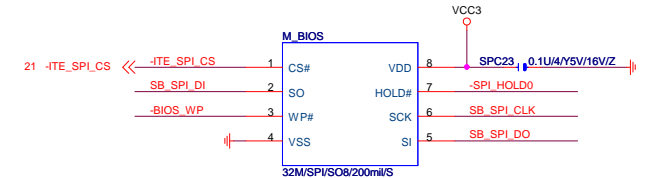
FC_CLK AH28
FC_FBCLKOUT AG28
FC_FBCLKIN AF28
FC_OE#/GPIO145 AF28
FC_AVD#/GPIO146 AG28
FC_WVE#/GPIO148 AF28
FC_CE1#/GPIO149 AF28
FC_CE2#/GPIO150 AE28
FC_INT1/GPIO144 AF28
FC_INT2/GPIO147 AH28
FC_ADQ0/GPIO128 AJ27
FC_ADQ1/GPIO129 AJ26
FC_ADQ2/GPIO130 AH25
FC_ADQ3/GPIO131 AG24
FC_ADQ4/GPIO132 AG23
FC_ADQ5/GPIO133 AH23
FC_ADQ6/GPIO134 AG24
FC_ADQ7/GPIO135 AF21
FC_ADQ8/GPIO136 AF21
FC_ADQ8/GPIO137 AH22
FC_ADQ10/GPIO138 AJ24
FC_ADQ11/GPIO139 AJ24
FC_ADQ12/GPIO140 AJ25
FC_ADQ13/GPIO141 AJ25
FC_ADQ14/GPIO142 AG25
FC_ADQ15/GPIO143 AH25

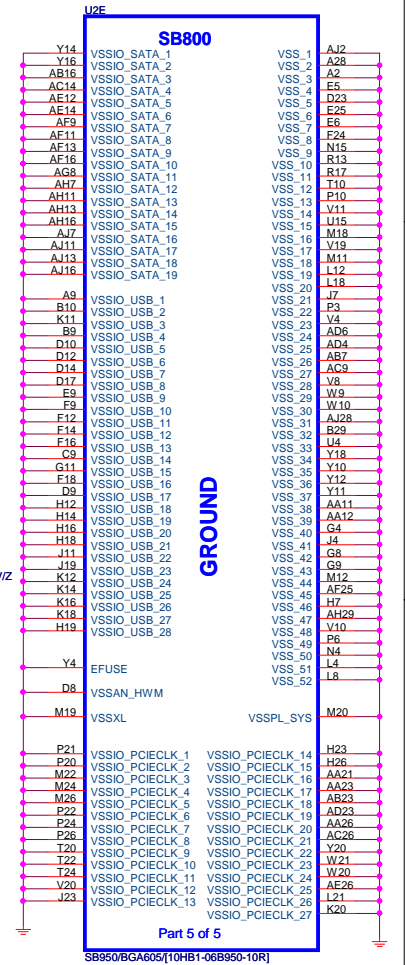
FANOUT0/GPIO52 W5
FANOUT1/GPIO53 Y9
FANOUT2/GPIO54 Y9
FANIN0/GPIO56 W7
FANIN1/GPIO57 W9
FANIN2/GPIO58 W8

TEMPIN0/GPIO171 B6
TEMPIN1/GPIO172 A6
TEMPIN2/GPIO173 A5
TEMPIN3/TALERT#/GPIO174 B5
TEMP_COMM C7

VIN0/GPIO175 A3
VIN1/GPIO176 B4
VIN2/GPIO177 A4
VIN3/GPIO178 C5
VIN4/GPIO179 A7
VIN5/GPIO180 B7
VIN6/GBE_STAT3/GPIO181 B8
VIN7/GBE_LED3/GPIO182 A8

SPI DI/GPIO164 NC1
SPI DO/GPIO163 NC2
SPI CLK/GPIO162 Y2
SPI CS#/GPIO165 Y2
ROM_RST#/GPIO161 Y2



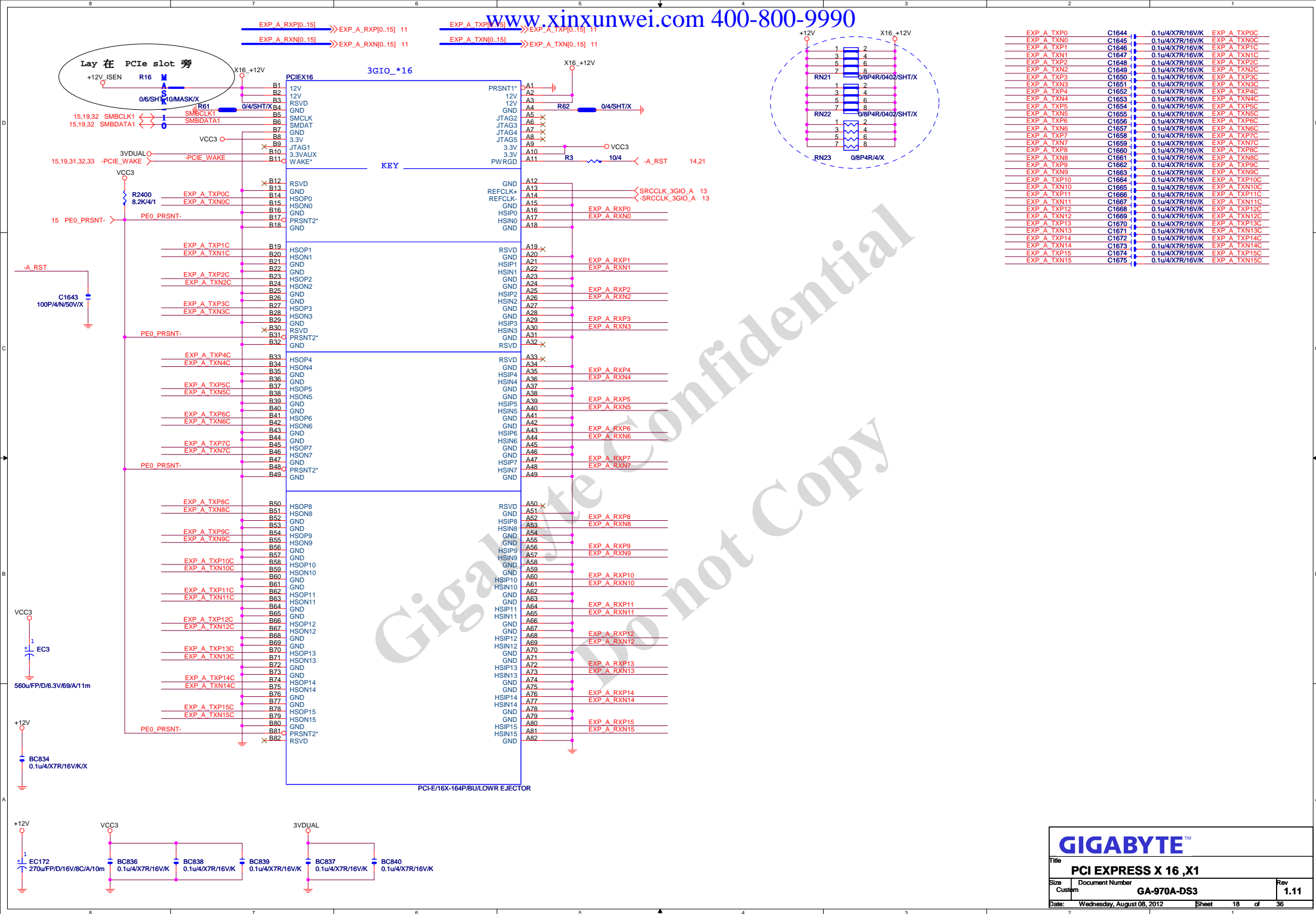


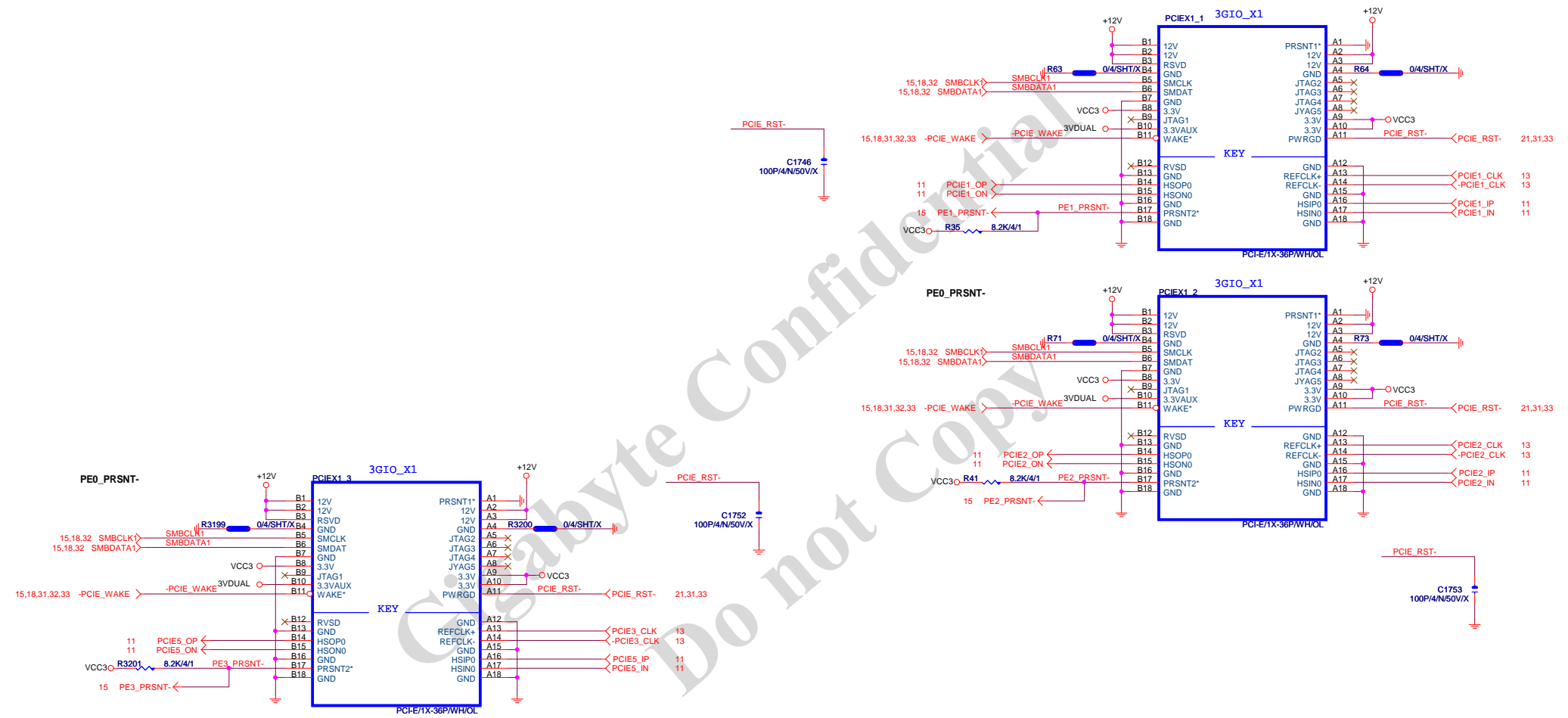
Part 5 of 5

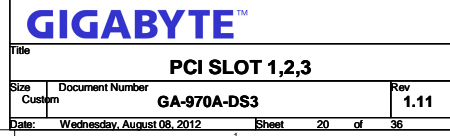
SB950/BGA605/[10HB1-06B950-10R]

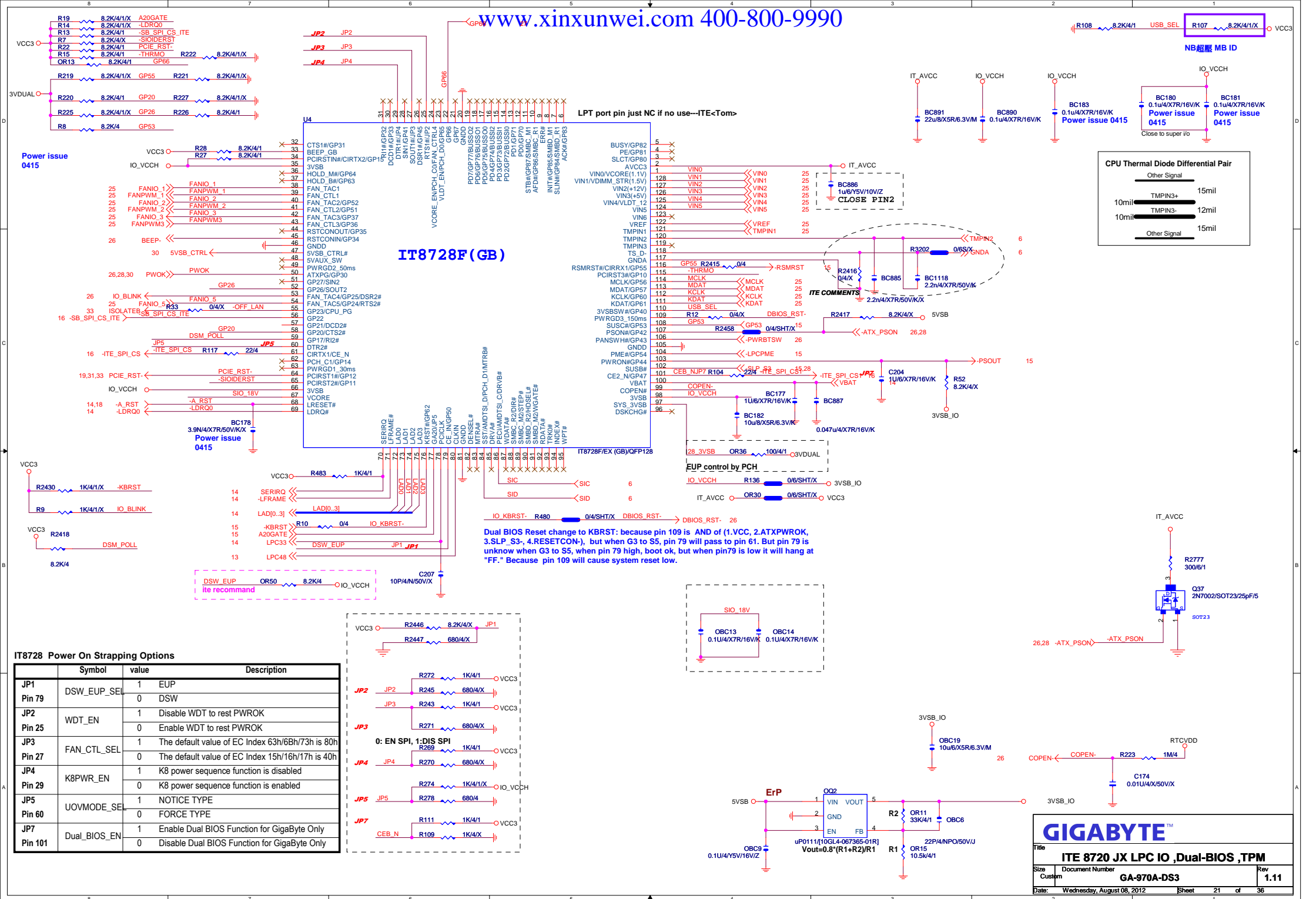
GIGABYTE™

Size Custom	Document Number GA-970A-DS3	Rev 1.11
Date: Wednesday, August 08, 2012	Sheet 17 of 36	

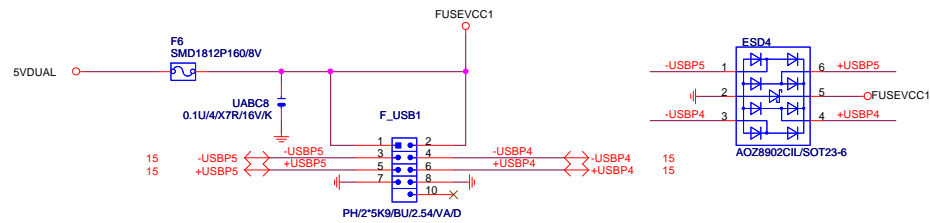




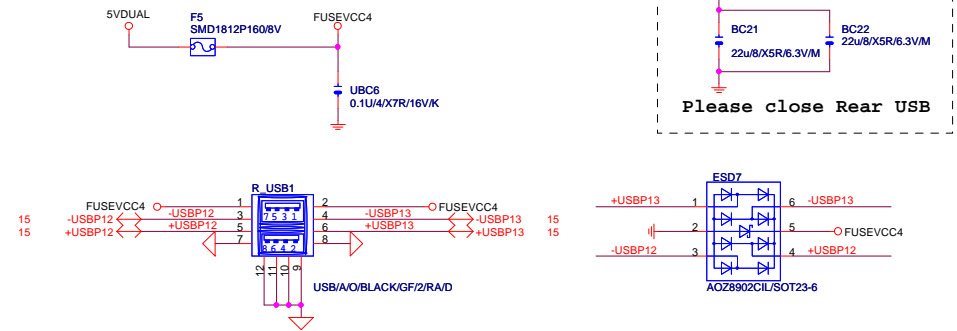




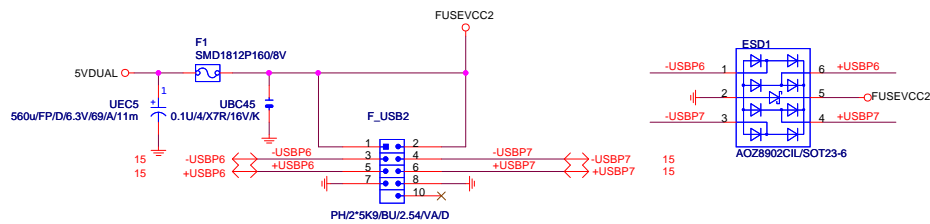
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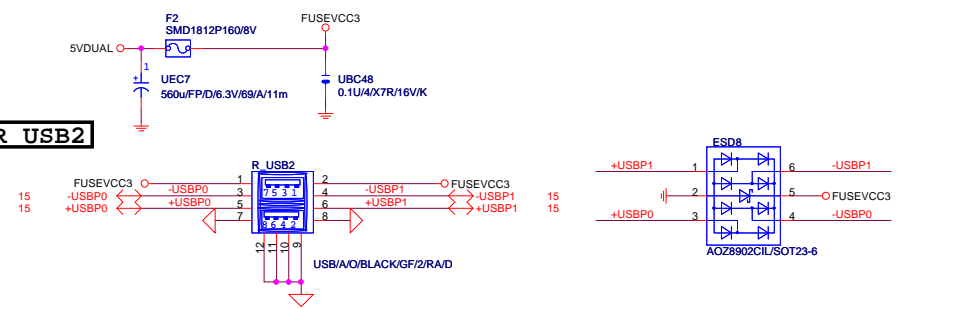
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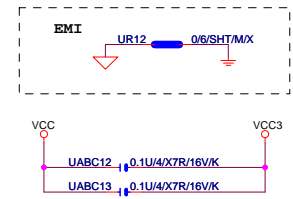
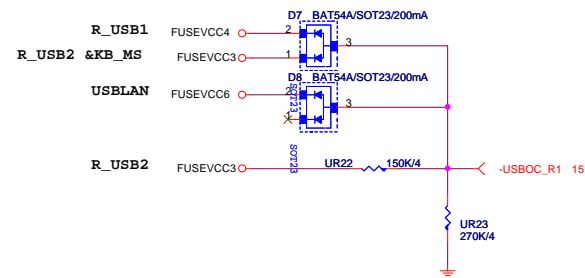
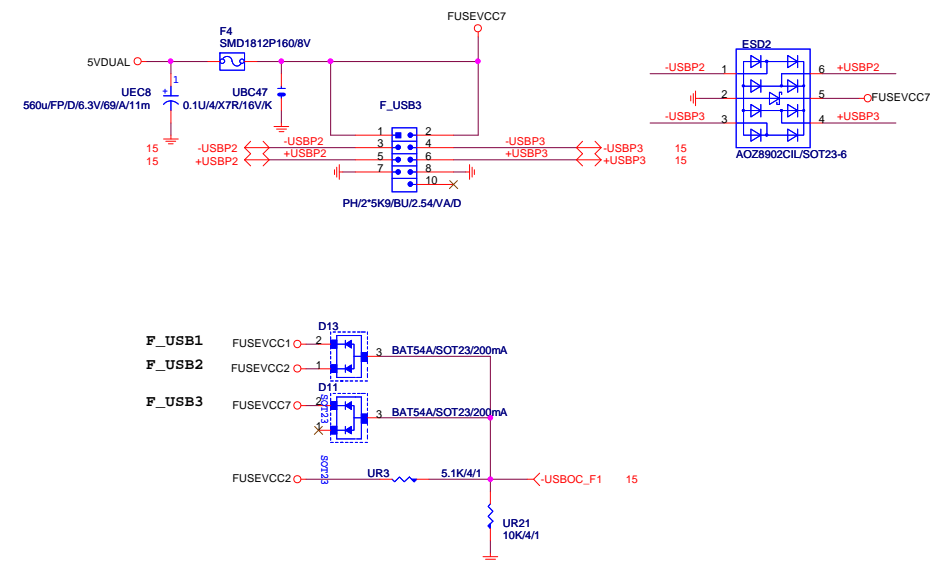
FRONT SIDE USB2



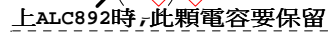
REAR USB2



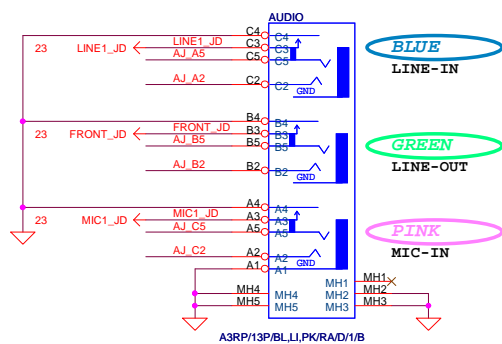
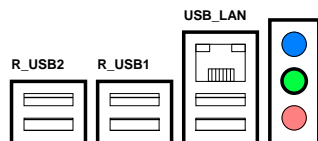
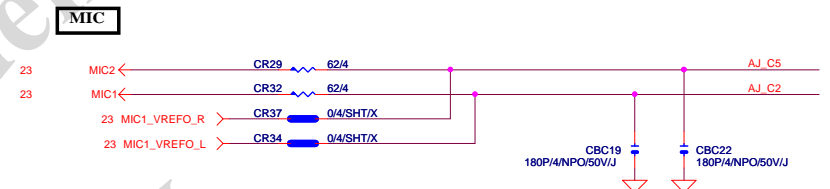
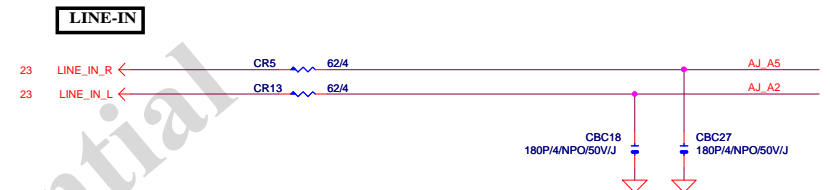
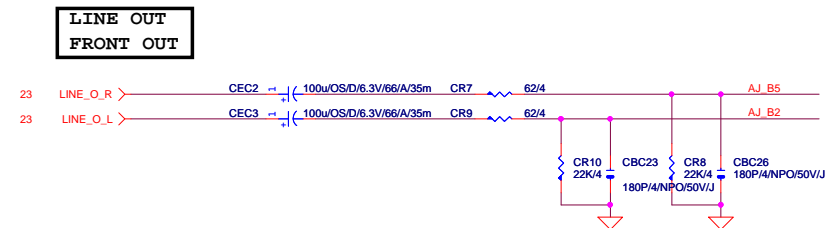
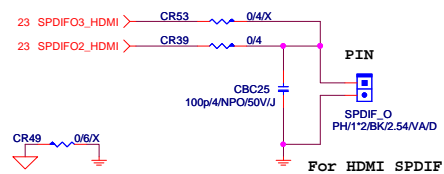
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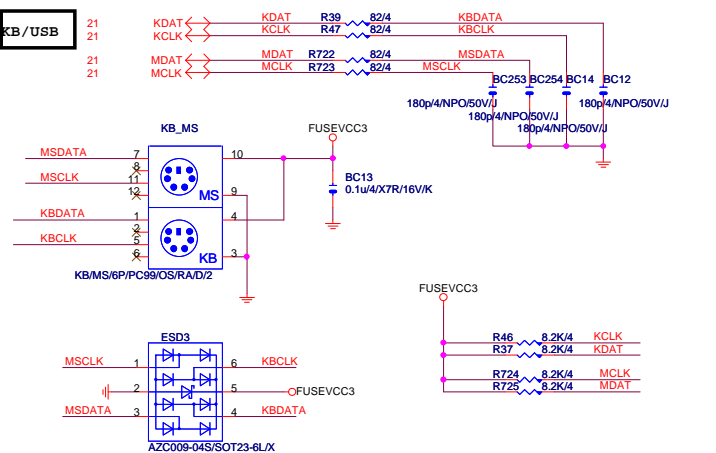
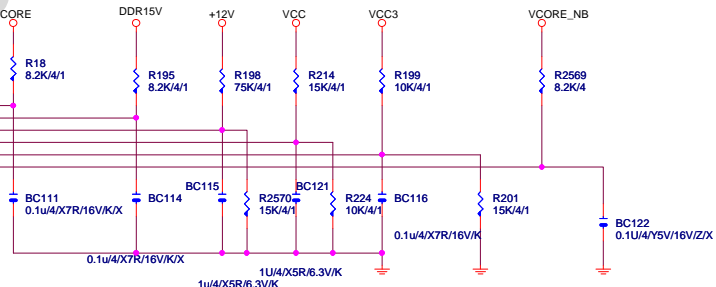
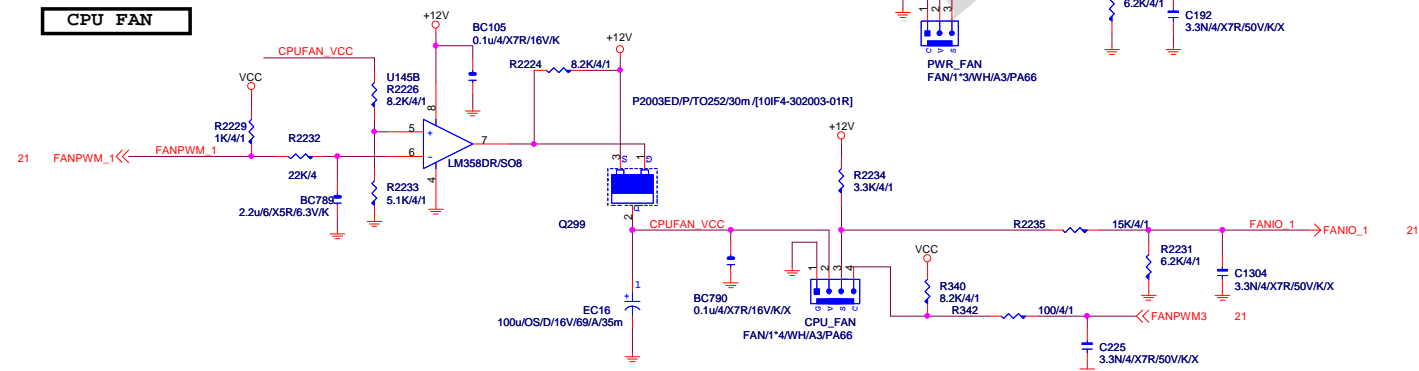
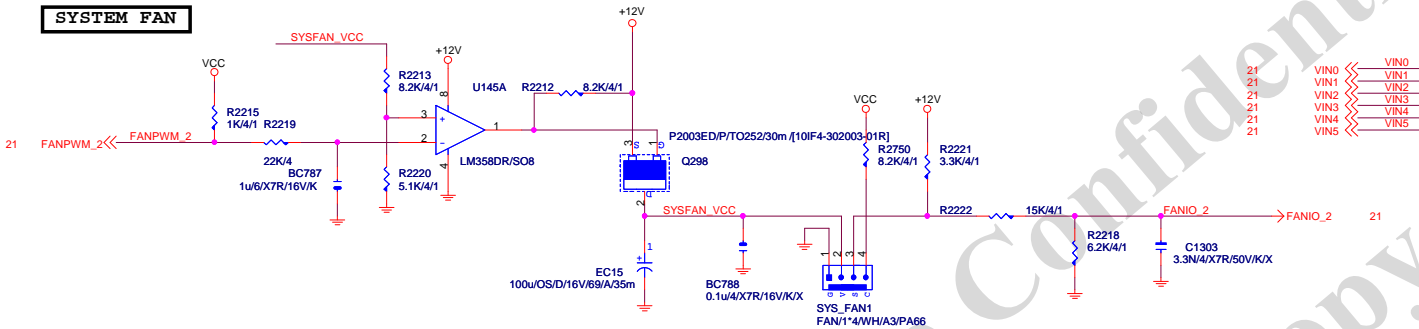
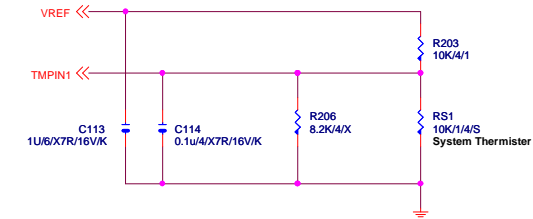


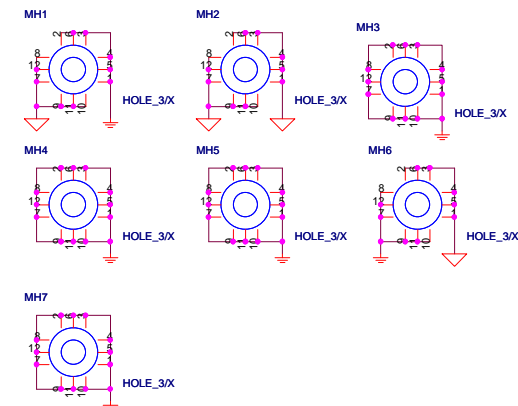
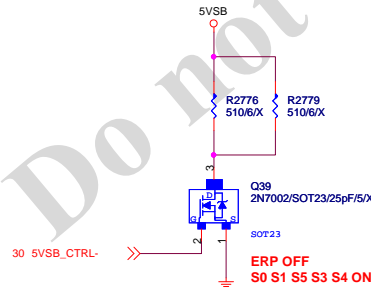
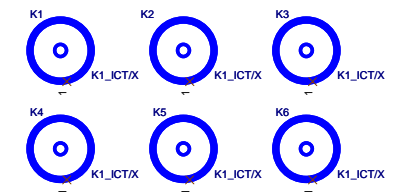
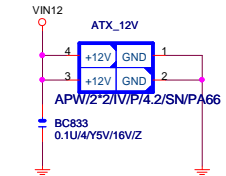
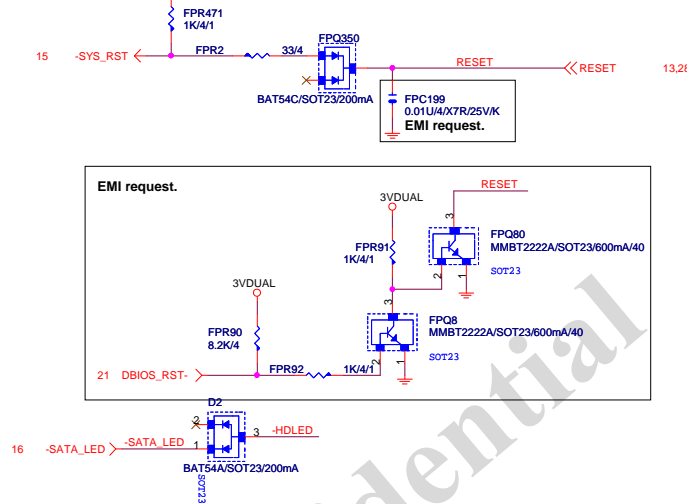
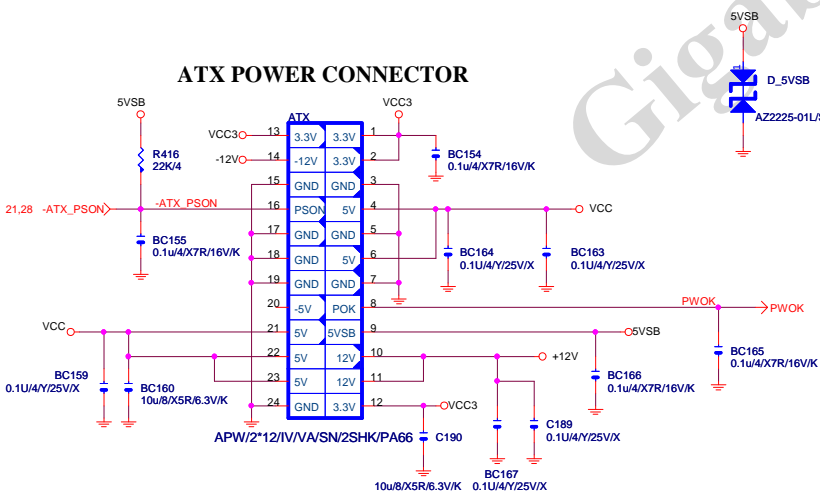
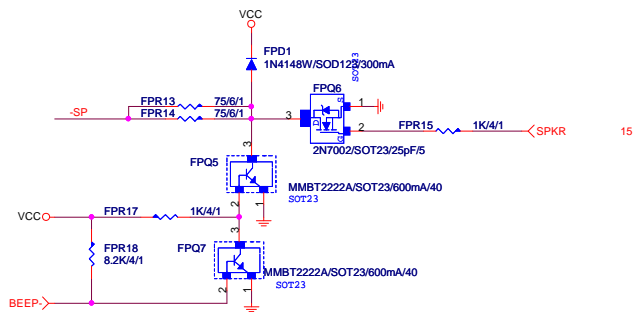
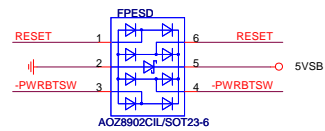
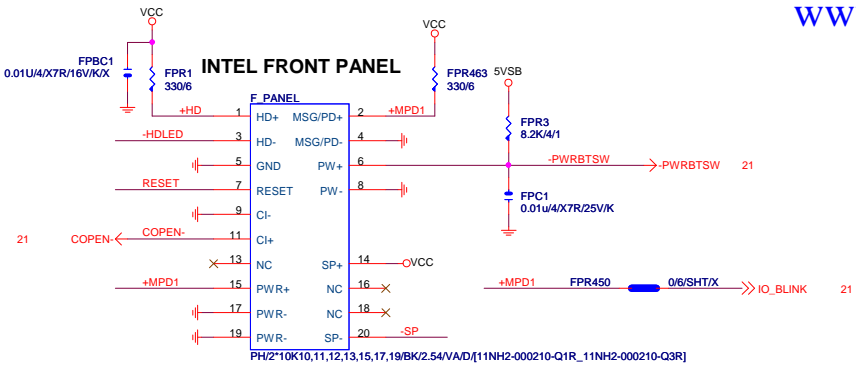


ADD CD2 For ESD PROTECT DIODE



Hardware Monitor circuits

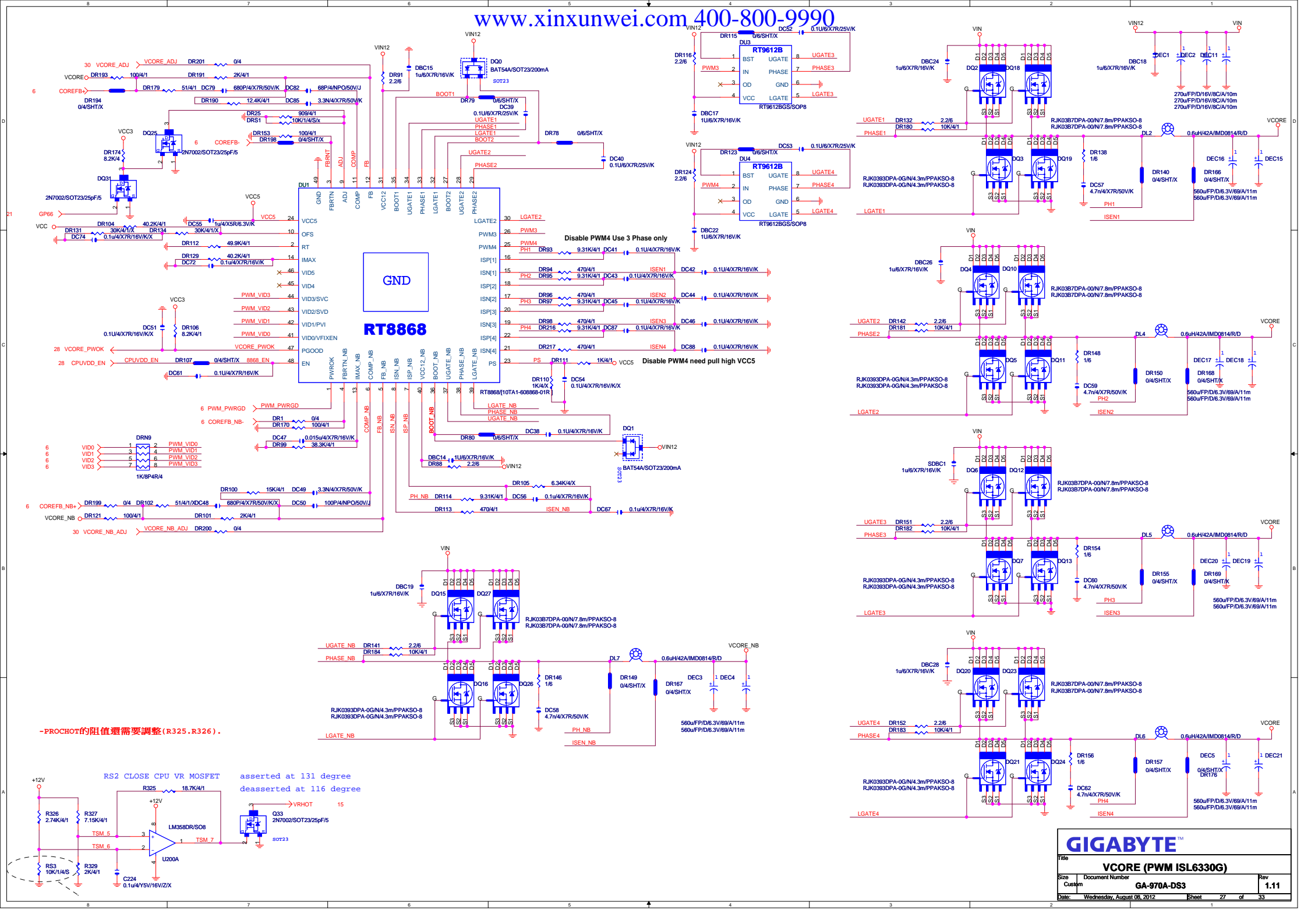


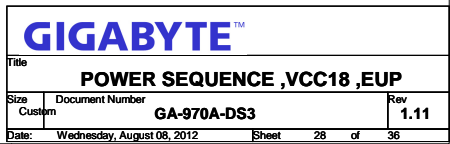


For Seasonic 900W
Power supply
cant Boot issue

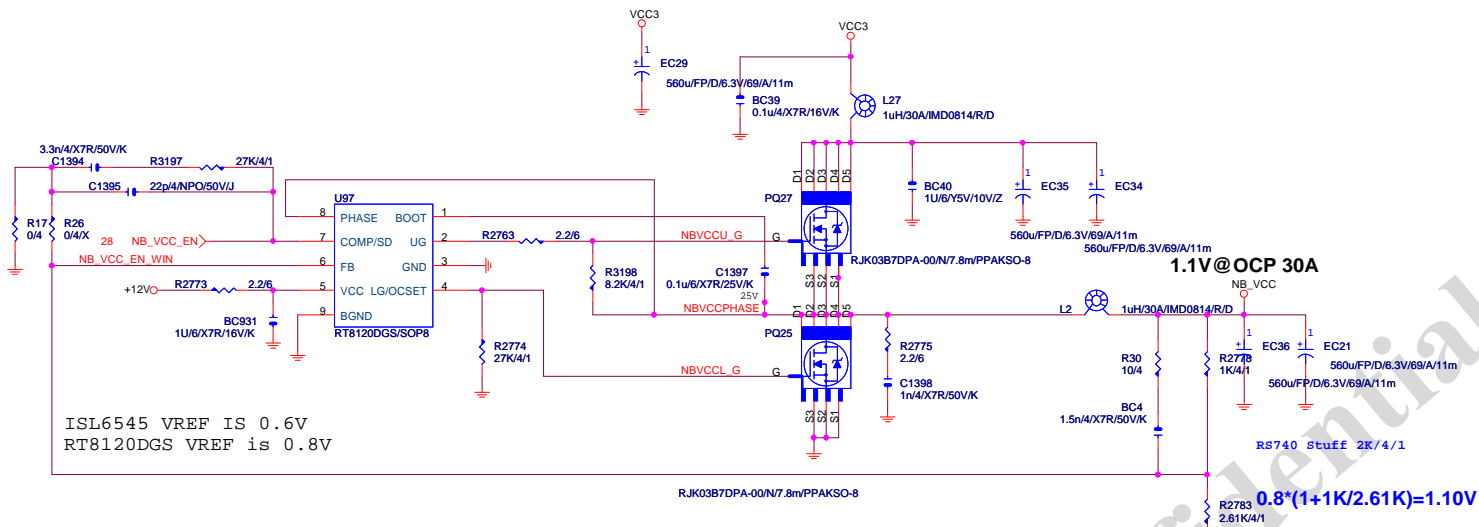
www.xinxunwei.com 400-800-9990

VCORE_ADJ 30
VCORE_ADJ 100K/1
COREFB- DR194 0.1u/4X7R/16V/K
DR179 51K/1
DR191 2K/4/1
DR190 12.4K/4/1
DC85 3.3K/4X7R/50V/K
DR25 909K/1
DR153 100K/4/1
DR196 0.1u/4X7R/16V/K
VCC3
DQ25 2N7002/SOT23/25pF/5
COREFB-
DR174 8.2K/4
DQ31 2N7002/SOT23/25pF/5
GP66
VCC
DR131 30K/4/1
DR134 0.1u/4X7R/16V/K
DR129 40.2K/4/1
DC72 0.1u/4X7R/16V/K
VCC3
DC51 0.1u/4X7R/16V/K
DR106 8.2K/4/1
VCC5
DR107 0.1u/4X7R/16V/K
DR108 8.2K/4/1
VCC5
DR109 0.1u/4X7R/16V/K
DR110 0.1u/4X7R/16V/K
DR111 1K/4/1
DR112 49.9K/4/1
DR113 470K/4/1
DR114 9.31K/4/1
DR115 0.1u/4X7R/16V/K
DR116 2.2/6
DR117 0.1u/4X7R/16V/K
DR118 0.1u/4X7R/16V/K
DR119 0.1u/4X7R/16V/K
DR120 0.1u/4X7R/16V/K
DR121 100K/4/1
DR122 0.1u/4X7R/16V/K
DR123 0.1u/4X7R/16V/K
DR124 0.1u/4X7R/16V/K
DR125 0.1u/4X7R/16V/K
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DR127 0.1u/4X7R/16V/K
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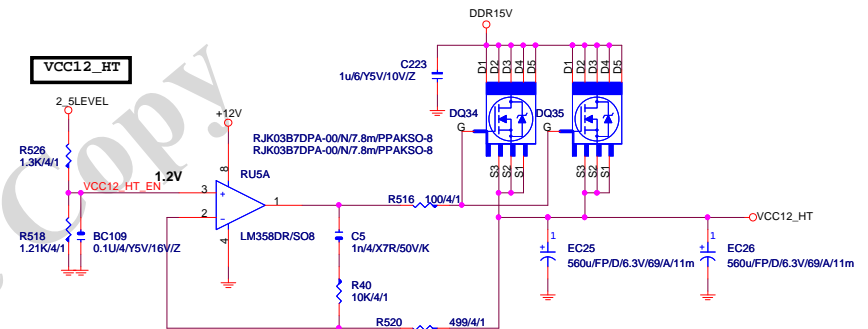




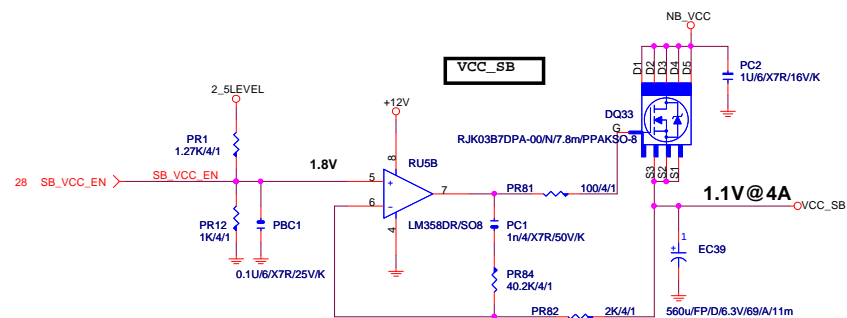
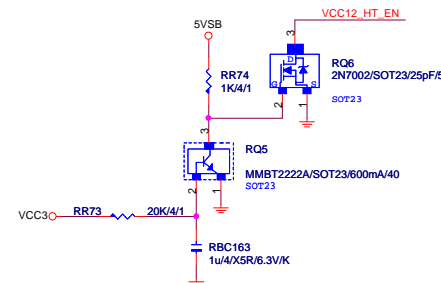
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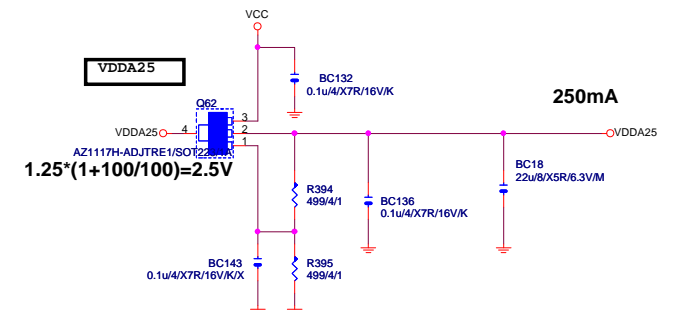
VCC12_HT



VCC_SB

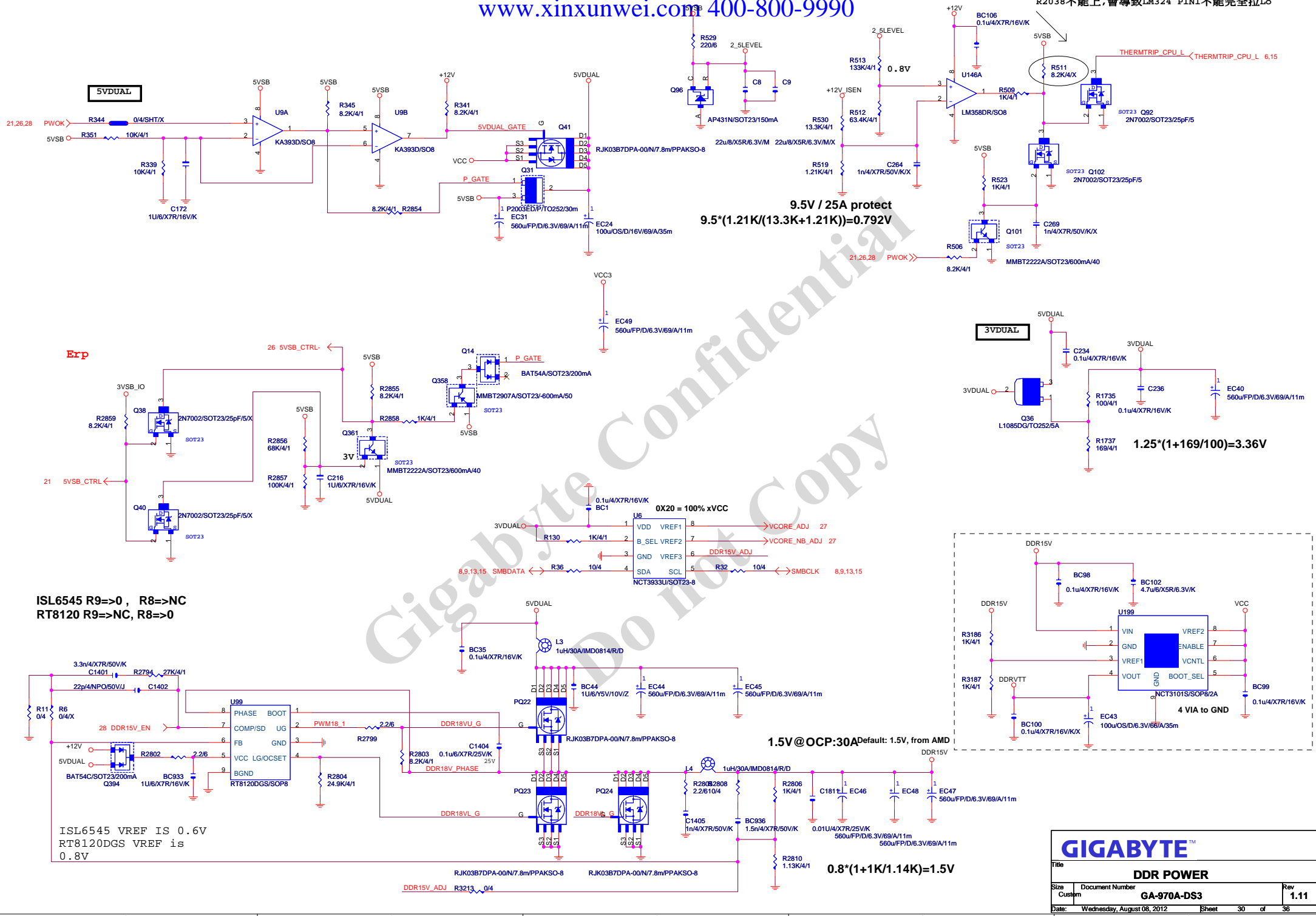
Patch AMD Validation
VDDA25 & VCC12_HT
power sequence

VDDA25

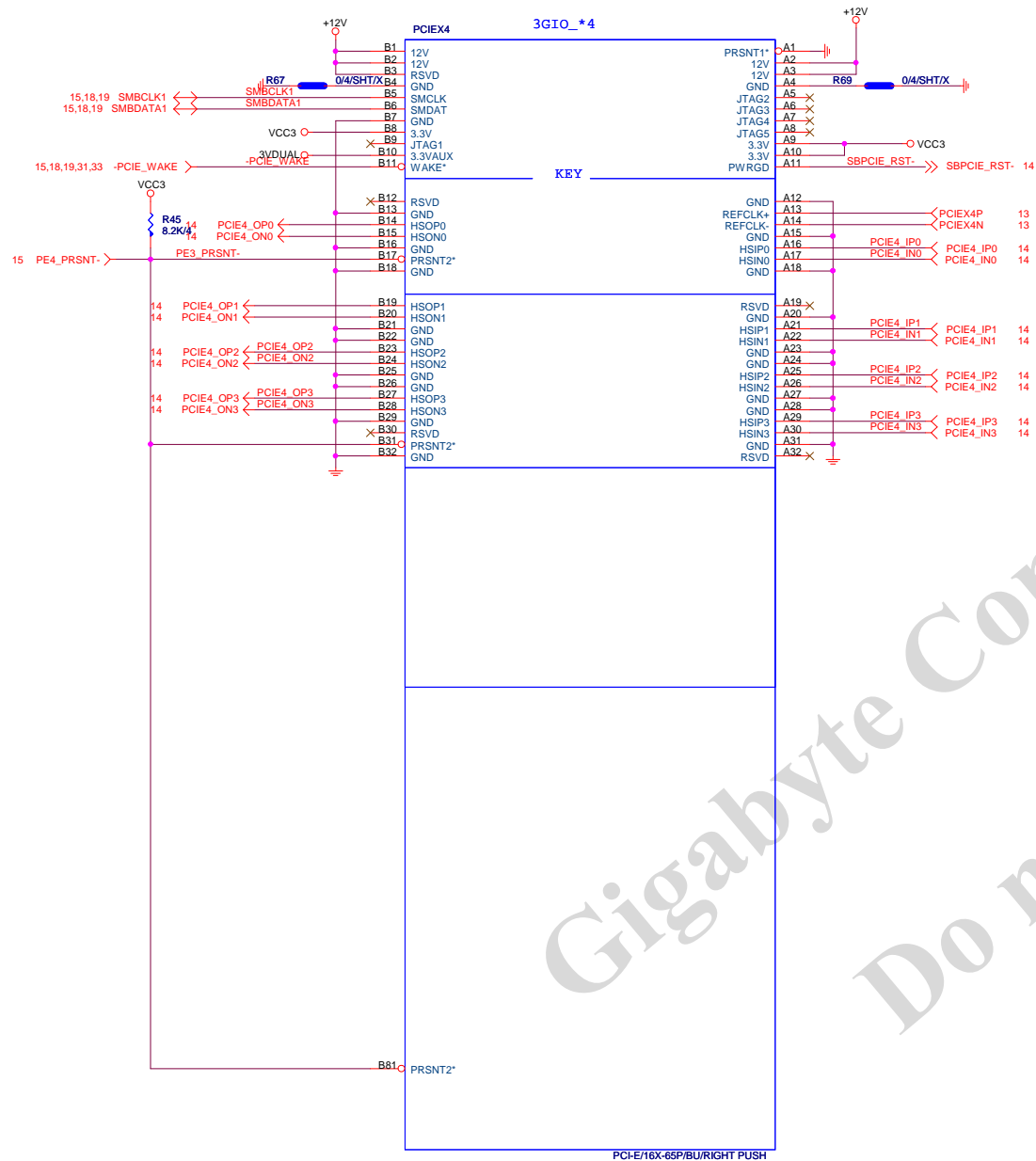


GIGABYTE™

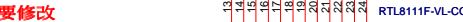
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NB/SB POWER, VCC12HT, VDDA25, VCC12Dual		
Size	Document Number	Rev
Custom	GA-970A-DS3	1.11
Date:	Wednesday, August 08, 2012	Sheet 29 of 36



Close to USB30_LAN
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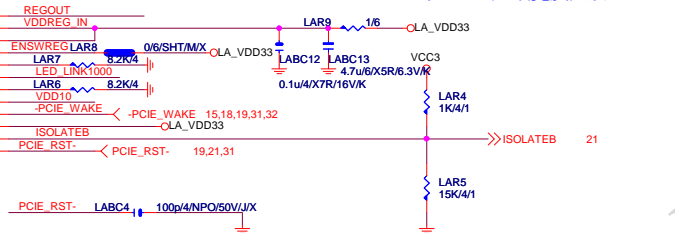


LA_VDD3

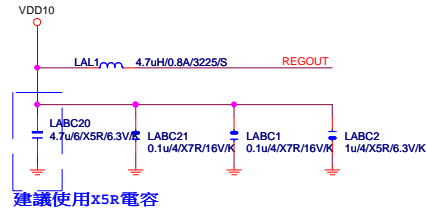
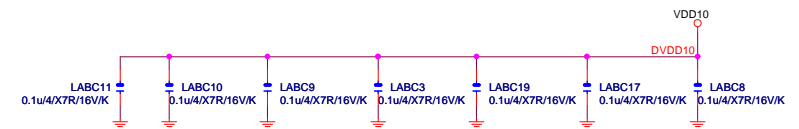
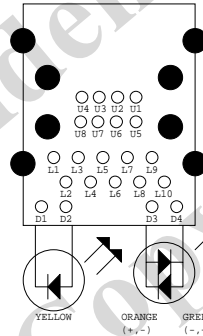


The diagram illustrates the electrical connections for the Close LAN chip. It features several input/output pins on the left and a central component labeled 'CLOSE LAN CHIP' with a note '離IC近越好 200mil以內' (Keep IC close, 200mil or less). The connections are as follows:

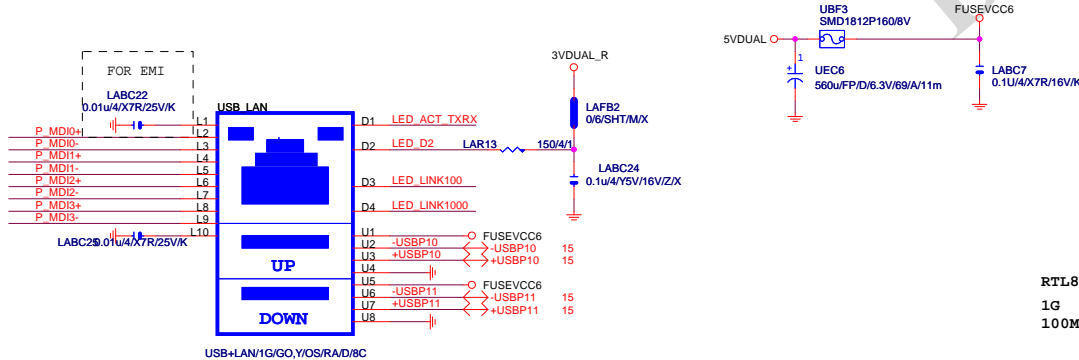
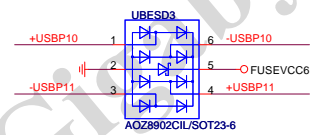
- 3VDUAL** is connected to **LA2** and **LA1** through resistors labeled **8.2K/4**.
- 11** is connected to **ML_OP** and **ML_ON**.
- 13** is connected to **SRCLK_LAN** and **-SRCLK_LAN**.
- 11** and **11** are connected to **ML_IP** and **ML_IN** through a resistor labeled **LC3**.
- 11** and **11** are connected to **ML_IP** and **ML_IN** through a resistor labeled **LC4**.
- There are two **0.1u/4X7R/16V/K** capacitors connected to the **ML_IP** and **ML_IN** lines.



P35-152-19W9



```
RTL8101E:LR38/LC5/LR43/LC6-->O
RTL8111C:LC6-->O
RTL8102E:LC5/LC6-->O
```



```
RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)
1G :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1
```

